

**National University**



of Computer

and

Emerging Sciences

Chiniot

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Faisalabad Campus



**EE1005 – Digital Logic Design**

**Quiz# 3**

**Instructor:** Muhammad Adeel Tahir **Section:** CS-2F **Time:** 20 Minutes

**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

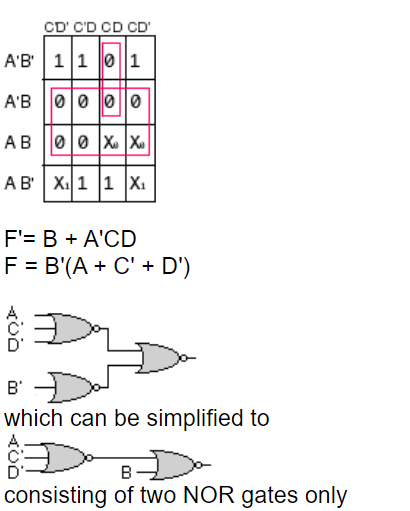
**Roll No: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Total: 10 marks**

***Note:*** *Use the back side of the page if needed. Make sure the handwriting is neat and clean while drawing the circuit, quiz will be marked as 0 if attempted in a writing that is not readable at all.*

**Q1: Implement the following Boolean function F together with the don't-care condition d using no more than two NOR gates. Assume that both the normal and complement inputs are available.**

**(10 marks)**

**Solution:**

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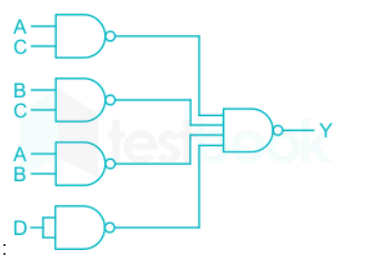
**Q2 Implement the following as two-level NAND only circuits:**

1. **(2.5 + 2.5 = 5 marks)**
2. **(2.5 + 2.5 = 5 marks)**

**a)**

**A white background with black text

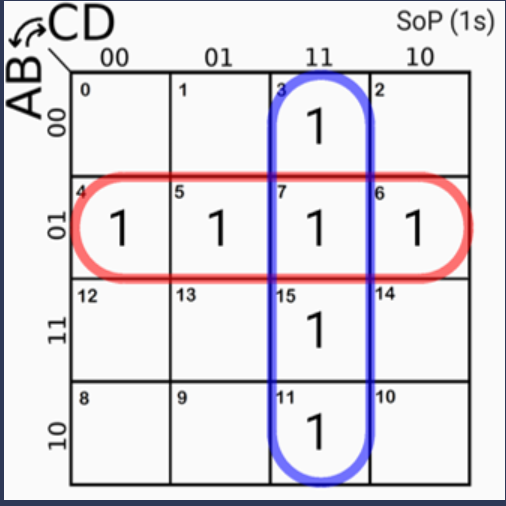
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**b)**

**F(A,B,C,D)=∑m(3,4,5,6,7,11,15)**

**Using the k-map as Sum of Product of the given function, we get**



**We need to make the circuit using only NAND gates for which we will :**

**Circuit diagram is as followed:**

**A diagram of a block

Description automatically generated**